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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/578,362

01/16/2007

Stefan Tasch

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08/05/2009

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EXAMINER

LOXAS, PETER J

ART UNIT

PAPER NUMBER

2811

MAIL DATE

DELIVERY MODE

08/05/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/578,362	TASCH ET AL.	
	Examiner	Art Unit	
	PETER LOXAS	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 26-47 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 26-47 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 5/5/2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>11/6/2007</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Status of Application

This office action is in response to the filing of the application papers on 05/05/2006. New claims 26-47 are pending in this application. Claims 1-25 have been cancelled by the pre-amendment filed 5/5/2006, without prejudice or disclaimer of subject matter.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 35-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 35 recites the limitation "plate" in line 5. There is insufficient antecedent basis for this limitation in the claim.

For examination purposes, claim 35 will be treated as: "...the substrate of the light-emitting diodes is towards the multilayer board."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 26-28, 35, and 38-47 are rejected as can be understood under 35 U.S.C. 103(a) as being unpatentable over Harrah, US Patent No. 6,498,355 B1.

RE CLAIM 26: Harrah teaches (fig. 3) a **light-emitting diode arrangement** (LED Array, abstract) **having:**

at least one light-emitting diode chip (28),

a multi-layer board (6, 8, 10) having a base (24) of a thermally well conducting material (24), in particular of metal (silver filled epoxy, col. 3, line 38), and an electrically insulating and thermally conducting connection layer (46, thermal contact, col. 4, line 55) between the emission surface of the light-emitting diode chips (28) and the board (6, 24), wherein between the light-emitting diode chip (28) and the board (6, 8, 10) there is arranged an intermediate carrier (30, submount) separate from those parts with which the light-emitting diode chip (28) is electrically contacted (Harrah states conventional reflowed solder bumps electrically connect a region of the LED to a top contact on submount).

Harrah teaches substantially the limitations of claim 1 as shown above. Harrah is silent as to **the intermediate carrier is formed by an aluminum nitride substrate.**

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ aluminum nitride substrates as intermediate carriers

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when good electrically insulating and thermally conductive properties are wished for.

RE CLAIM 27: Harrah teaches (fig. 3) **the electrically insulating connection layer (46) is at least the boundary surface (46) of the light-emitting diode chip (28) which is towards the board (6, 8, 10)** (Harrah states that the dielectric layer is optional (col. 4, line 60)).

RE CLAIM 28: Harrah teaches (fig. 3) **the electrically insulating connection layer (46) is at least an adhesive layer (46, solderable metal layers, col. 4, lines 64-65).**

RE CLAIM 35: Harrah teaches (fig. 3) **the light-emitting diode chip (28) is so arranged that the substrate of the light-emitting diodes (28) is towards the plate (6, 8, 10).**

RE CLAIM 38: Harrah teaches (fig. 3) **the light-emitting diode chip (28) is so arranged that the substrate (bottom surface) of the light-emitting diodes (28) is away from the board (6, 8, 10)** (The substrate of the light-emitting diodes are away from the board (see MPEP 2111)).

RE CLAIM 39: Harrah teaches (fig. 3) **the light-emitting diode chip (28) is arranged on the intermediate carrier (30) by means of a conductive adhesive**

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(solder, col. 4, line 40).

RE CLAIM 40: Harrah teaches (fig. 3) **the side of the intermediate carrier (30) towards the board (6, 8, 10) is electrically insulating** (ceramic, col. 4, line 39).

RE CLAIM 41: Harrah teaches (fig. 3) **the region of the intermediate carrier (30, submount) towards the light-emitting diode chip (28) has conductive regions** (silicon, col. 4, line 39).

RE CLAIM 42: Harrah teaches (fig. 3) **at least the region of the light-emitting diode chip (28) is covered by a lens (26).** However, Harrah is silent as to the lens in particular a Fresnel lens (9).

It would have been obvious to a person of ordinary skill in the art to employ a Fresnel lens in order to cover a plurality of LED dies. It is well known in the art that multiple types of lenses could perform the equivalent function of covering a plurality of LED dies.

CLAIM 43: Harrah teaches (fig. 3) **the region between the board (6, 8, 10) and the lens (26) is at least partially filled by a material** (Harrah states small portions of clear material may be conventionally dispensed onto some or all of the LED and then cured to form simple lenses (col. 4, line 5-8). **However, Harrah is silent as to the material is a colour conversion material.**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a colour conversion material between the board and the lens, since it has been held to be within the general skill of a worker in the art to select known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

RE CLAIM 44: Harrah teaches **the material is arranged above and alongside the light emitting diode chip** (Harrah states small portions of clear material may be conventionally dispensed onto some or all of the LED and then cured to form simple lenses (col. 4, line 5-8). However, Harrah is silent as to the material is **a colour conversion material**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a colour conversion material between the board and the lens, since it has been held to be within the general skill of a worker in the art to select known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

RE CLAIM 45: Harrah teaches (fig. 3) **the light emitting diode chip (28) is contacted (through solder bumps) by a circuit board (8, trace layer) by means of wires (48, 50), and the circuit board (8) is applied to the board (6, 8, 10) sandwich-like by means of an insulating layer (10, dielectric layer) lying therebetween.**

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CLAIM 46: Harrah teaches (fig. 3) **at least one light emitting diode chip (28), a multi-layer board (6, 8, 10), having a base of a thermal well conductive layer (24), in particular of metal (silver filled epoxy); and**

an electrically insulating and thermally conducting connection layer (46) between an emission surface of the light-emitting diode chip (28) and the board (6, 8, 10), wherein between the light-emitting chip (28) and the board (6, 8, 10) there is arranged an intermediate carrier (30) separate from those parts with which the light-emitting diode chip (28) is electrically contacted.

Harrah shows substantially the limitations of claim 46 as shown above. Harrah is silent as to **a colour conversion material is arranged above and alongside the light-emitting diode chip.**

RE CLAIM 47: Harrah teaches (Fig. 3) **at least on light-emitting diode chip (28); a multilayer board (6, 8, 10), having a base of a thermally well conducting layer (24), in particular of metal (silver filled epoxy, col. col. 3, line 38); and**

an electrically insulating and thermally conducting connection layer (46) between an emission surface of the light-emitting diode chip (28) and the board (6, 8, 10), wherein between the light-emitting chip (28) and the board (6, 8, 10) there is arranged an intermediate carrier (30) separate from those parts with which the light-emitting diode chip (28) is electrically contacted, and wherein the

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light-emitting diode chip (28) is arranged on the intermediate carrier (30) by means of a conductive adhesive (solder).

Claims 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrah, and further in view of Hashimoto et al. (Hashimoto) US Pub. No. 2004/0065894 A1.

Harrah shows substantially the limitations of claim 26 as shown above. Harrah is silent as to the depression of the board.

RE CLAIM 29: However in an analogous structure, Hashimoto shows (fig. 18A) **the light-emitting diode chip (1) is accommodated in a depression (13, insertion hole, ¶ 52) of the board (12, ¶ 48).**

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ a depression to accommodate the LED chip as shown by Hashimoto in order to insert the projection of the metal plate respectively (¶ 52).

CLAIM 30: Hashimoto teaches (Fig. 11) **the light-emitting diode chip (1) is arranged in the region of a depression (11b, housing recess, ¶ 48) in the base material (11, ¶ 48) of the board (12).**

CLAIM 31: Hashimoto teaches (fig. 11) **the light-emitting diode chip (1) does not project beyond the contour of the board (12).**

CLAIM 32: Hashimoto teaches (fig. 11) **the light-emitting diode chip (1) ends plane with the upper side of the board (12).**

CLAIM 33: Hashimoto teaches **the depression (11b) has the function of the reflector** (Hashimoto states that the side wall of the housing recess that is part of the metal plate functions as a reflector (abstract)).

CLAIM 34: Hashimoto teaches (fig. 11) **the walls (11a) of the depression (11b) are at least partially beveled** (as seen in figure 11).

CLAIM 36 & 37: Harrah teaches **the light emitting diodes (28).** However, Harrah is silent as to the substrate of the light-emitting diodes is of an electrically insulating material, such as sapphire.

However, in an analogous structure, Hashimoto teaches that conventional are shows **the substrate of the light-emitting diodes is formed of sapphire (¶ 2).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a substrate of the LEDs formed of an electrically insulating material, such as sapphire, since it has been held to be within the general skill

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of a worker in the art to select known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Cited Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reference 1: U.S. Patent No. 6,139,171 (Waldmann)

Waldmann discloses evidence of the level of ordinary skill in the art of a Fresnel lens wherein a plurality of LEDs are positioned behind said Fresnel lens.

Reference 2: U.S. Patent No. 2001/0001207 A1 (Shimizu et al.)

Shimizu et al. discloses evidence of the level of ordinary skill in the art of a lens and/or coating containing a color converting material.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PETER LOXAS whose telephone number is (571)270-7380. The examiner can normally be reached on IFP.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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7/23/09